# Improved reticle requalification accuracy and efficiency via simulation-powered automated defect classification

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## ABSTRACT

Advanced IC fabs must inspect critical reticles on a frequent basis to ensure high wafer yields. These necessary requalification inspections have traditionally carried high risk and expense. Manually reviewing sometimes hundreds of potentially yield-limiting detections is a very high-risk activity due to the likelihood of human error; the worst of which is the accidental passing of a real, yield-limiting defect. Painfully high cost is incurred as a result, but high cost is also realized on a daily basis while reticles are being manually classified on inspection tools since these tools often remain in a non-productive state during classification.

An automatic defect analysis system (ADAS) has been implemented at a 20nm node wafer fab to automate reticle defect classification by simulating each defect's printability under the intended illumination conditions. In this paper, we have studied and present results showing the positive impact that an automated reticle defect classification system has on the reticle requalification process; specifically to defect classification speed and accuracy. To verify accuracy, detected defects of interest were analyzed with lithographic simulation software and compared to the results of both AIMS™ optical simulation and to actual wafer prints.

**Keywords:** ADC, automatic defect classification, freeform illumination, AIMS, defect printability, wafer, CD, reticle, photomask

## 1. INTRODUCTION

Manufacturing of logic devices, especially in a foundry business environment, results in many products manufactured with single mask sets. Maximizing the availability of these reticles in a high volume manufacturing environment is one of the critical aspects to meeting customer shipment demands. In addition, ensuring the quality of these reticles is paramount. The fast pace of MOSFET scaling is accelerating the introduction of smaller technology nodes extending CMOS beyond 20nm. These requirements are resulting in reticles with higher feature densities, smaller feature sizes and highly complex Optical Proximity Correction (OPC) which all contribute to an increase in the rate of false detections during reticle inspection. Higher false detections slows reticle requalification throughput and increases the chances of misclassified defects. In addition, imaging the smaller and more complex structures requires more flexibility in the illumination pupil on the exposure tool. Freeform illumination allows the pupil to be customized with the mask design beyond the limits of standard pupil-shaping optics, but is difficult to emulate with a reticle inspection tool. These rapid changes are creating a need to enable the Fab reticle engineers to disposition a reticle with high speed and quality, and this paper focuses on how to successfully address these issues.

## 2. MOTIVATION

The motivation was twofold: first, to have a method to prevent human errors from passing printable reticle defects affecting wafer production, and second, to create a model for reliable defect simulations, especially for 20nm reticles using freeform illumination, enabling fab reticle engineers to pass defects that will not print. Uncertainty on how to disposition a questionable reticle defect can lead to a decision to clean/repel a reticle, perform a wafer print test, or even

have a repair made back at the mask shop on a reticle that is actually fine to release to production. These options all cost time and money. Figure 1 shows the impact of holding and modifying production-ready reticles that should simply be released to production.

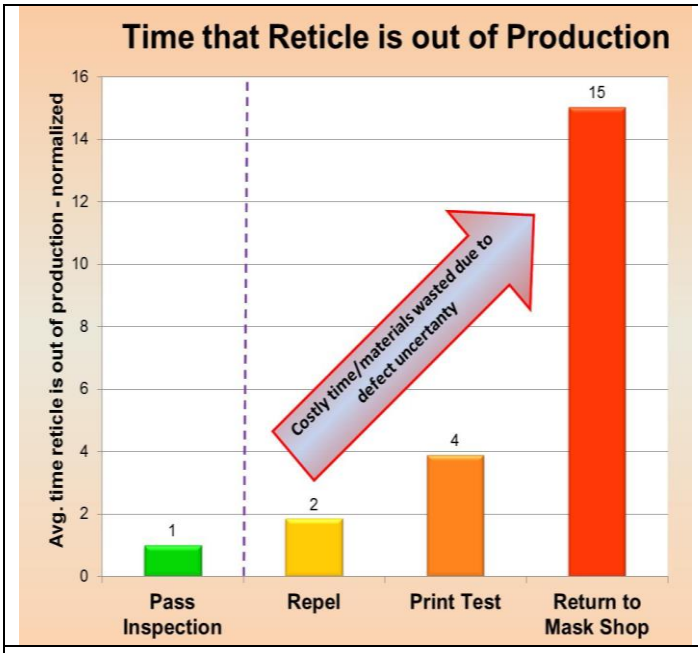


Figure 1: The time and cost impact of holding and modifying production-ready reticles

## 3. DATA FLOW

Automatic Defect Analysis System (ADAS) is a PC-based software product that automatically analyzes results from reticle inspection tools, classifying the defects with simulated wafer impact. It quickly classifies defects, separating false from real, allowing the operators to focus only on defects of concern.

ADAS also simulates how the defects will affect the wafer CD to help remove classification doubt. Figure 2 shows the data flow on how the server interfaces with other systems in the wafer fab. The server scans reticle inspection tools looking for new or updated inspections and downloads the inspection results. The inspections are then analyzed in seconds, and results are then available for operators to verify using in-fab review stations. Engineers and managers can also view or change results on any Windows-based computer at their desks.

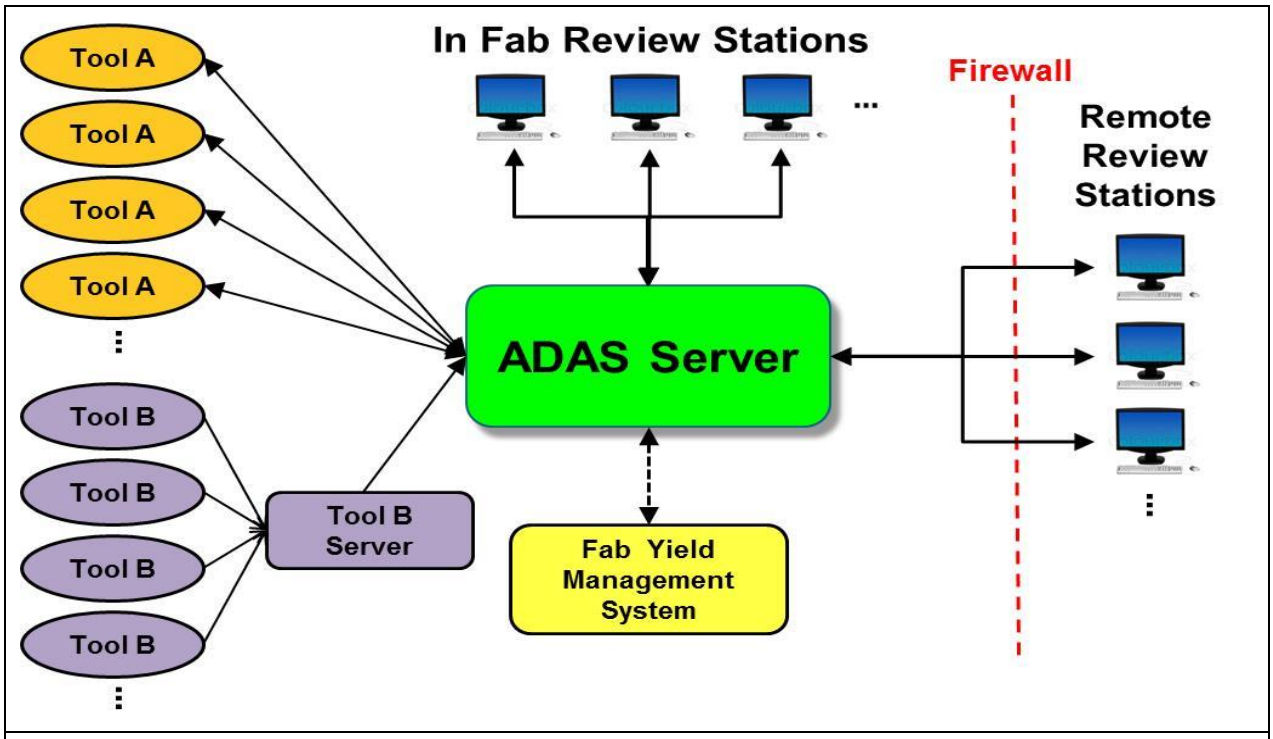


Figure 2: ADAS data flow path

## 4. AIMS VERIFICATION - 28NM NODE AND ABOVE

It is important to verify the results of this simulation software against the current industry accepted reticle defect analysis tools. This was done using an AIMS™ aerial image analysis tool on numerous defects. Figure 3 below shows an example of three production reticle defects that were analyzed by both AIMS and ADAS. Defects A and B, which are near the critical 10% CD error threshold, are examples of how ADAS matches more closely to AIMS in this critical region. Defect C is an example of how ADAS tends to exaggerate the impact of defects especially over 10% CD error. Exaggerating defect impact in this area can be compensated for, and in general is not critical, since defects of this size need to be cleaned or repaired in most cases.

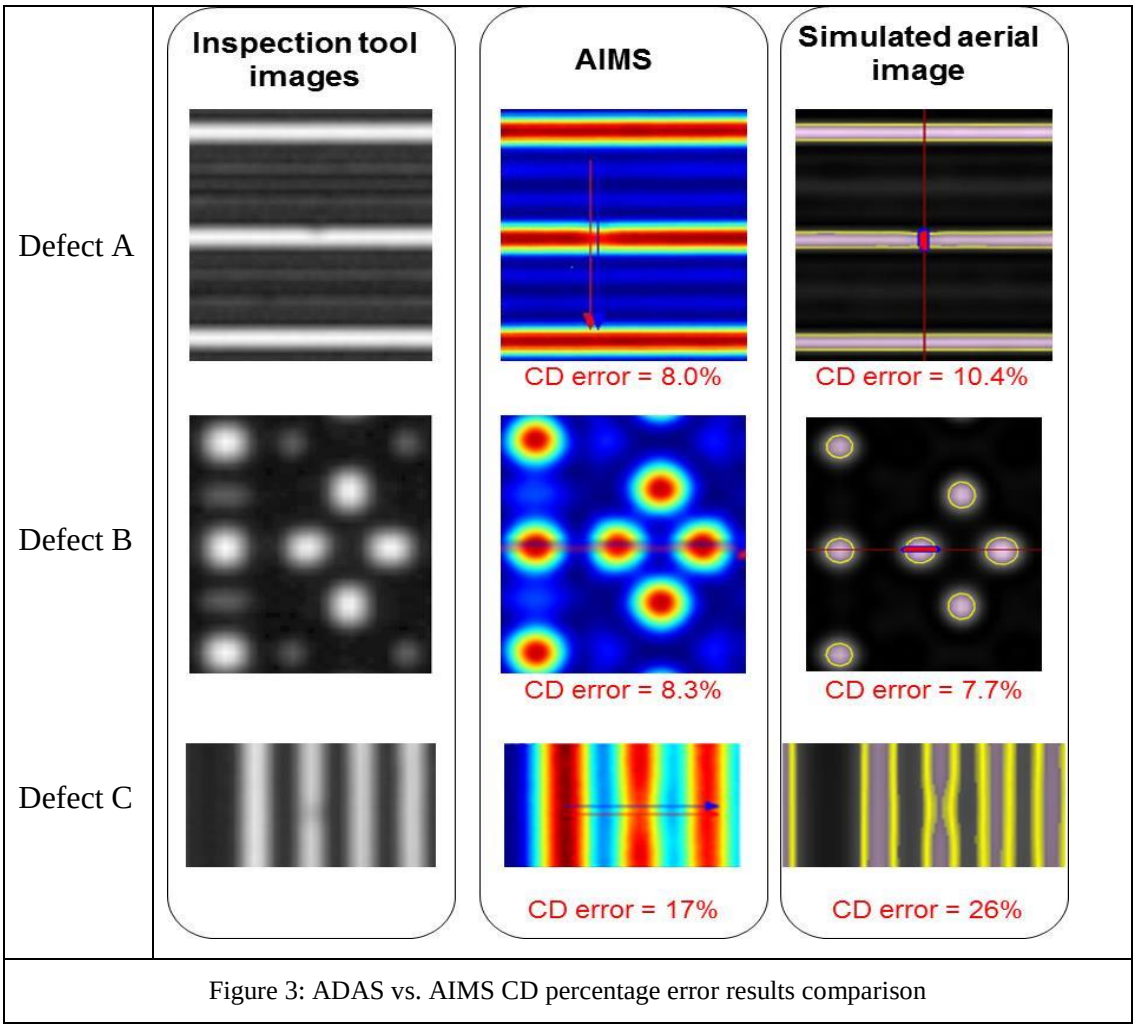


Figure 3: ADAS vs. AIMS CD percentage error results comparison

Past work in a 28nm memory fab has shown that ADAS simulation results match well with AIMS data at 28nm and above with a slight exaggeration as shown in Figure 4 **[1]**.

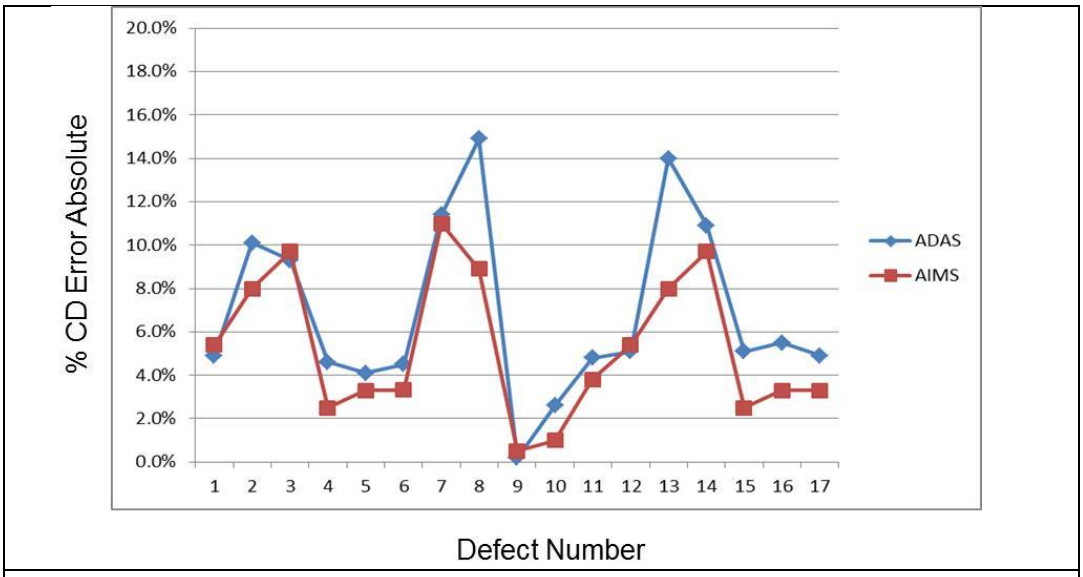


Figure 4: ADAS vs. AIMS simulation on naturally occurring defects

Current data also show good correlation with 28nm node and above naturally occurring defects (see Figure 5), noting the trend of ADAS to overestimate CD errors especially with larger reticle defects.

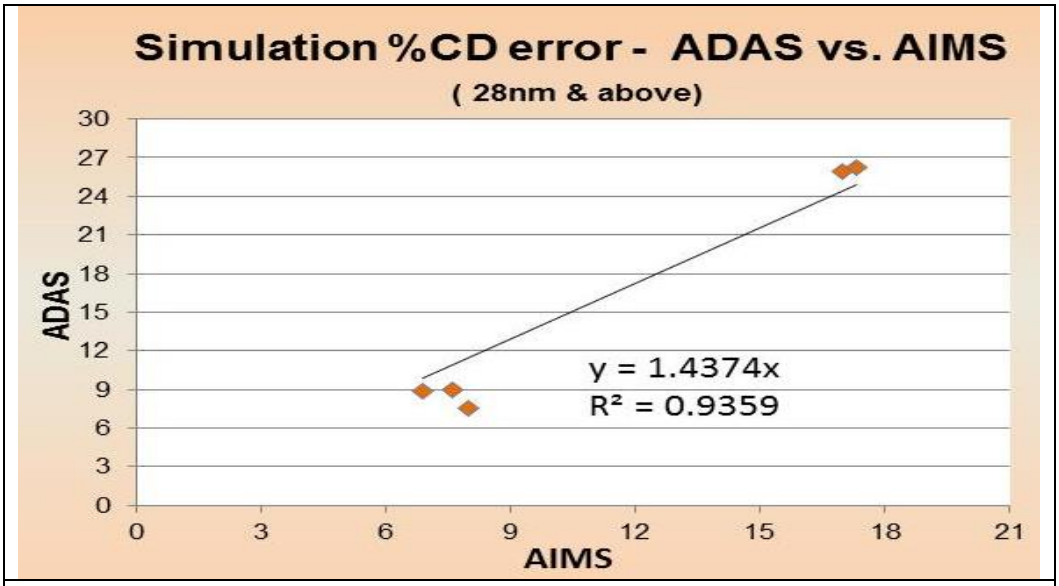


Figure 5: ADAS vs. AIMS CD percentage error results comparison

## 5. EFFICIENCY GAINS – THROUGHPUT AND SPEED

Automatic defect classification can significantly increase inspection tool productivity. Figure 6 shows that the average reticle inspection tool throughput increased 8.6% inspections per day averaged over the eight months evaluated after the release of ADAS **[1]**.

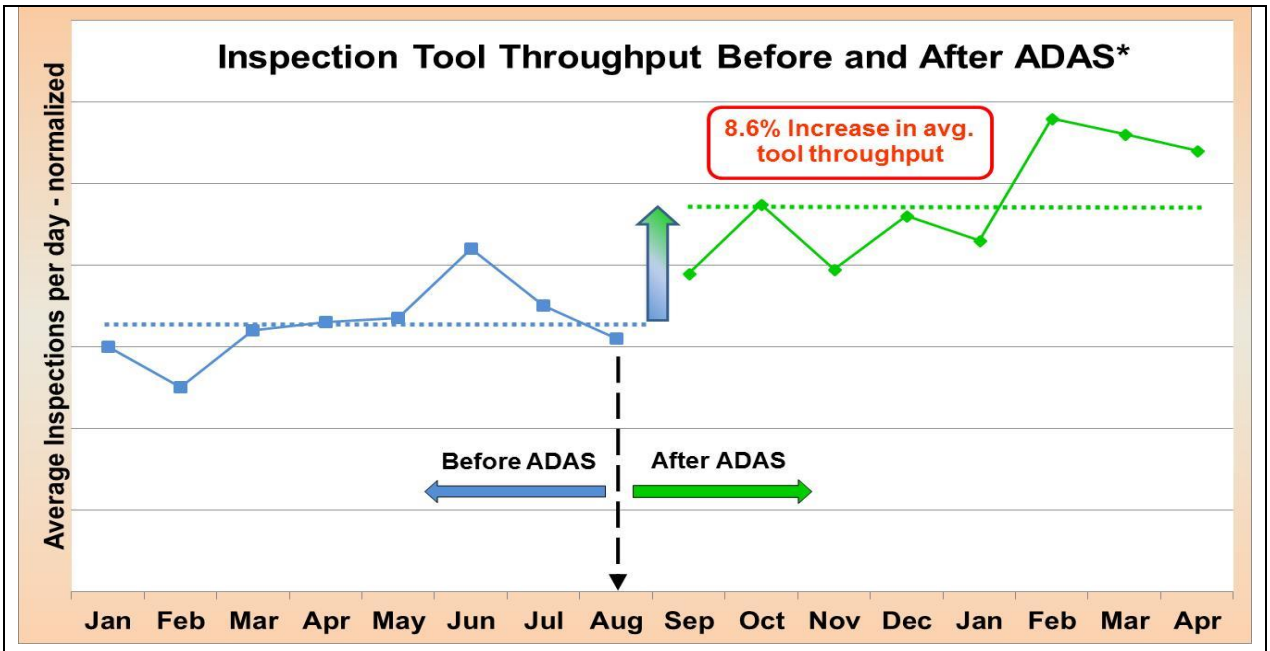


Figure 6 : A significant increase in inspection output seen after ADAS implementation

Figure 7a shows how reliable defect simulation provides engineers the confidence to release ∼50% more reticles with non-printing defects directly back to production, reducing the time and cost associated with unnecessary clean/repel, print checks, etc. Figure 7b shows how the combination of reliable defect classification and simulation has reduced the amount of time that engineers spend reviewing defects by ∼90%.

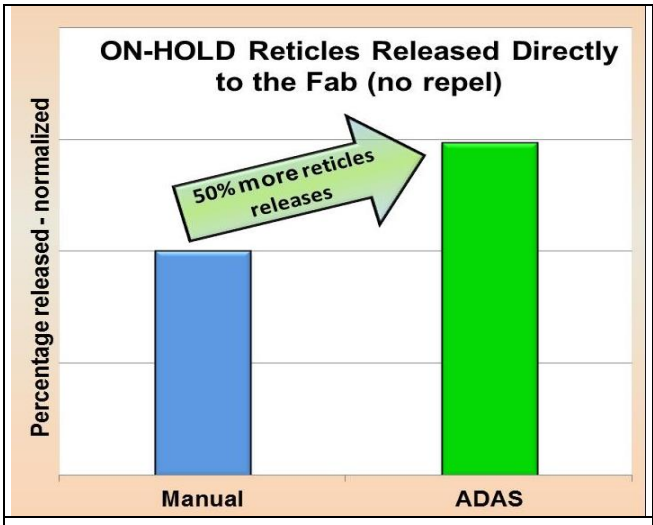


Figure 7a: Reliable simulation allows release of ∼50% more reticles

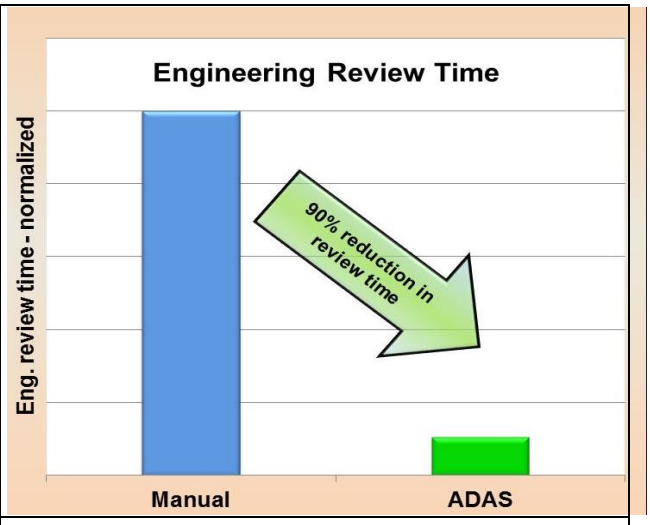


Figure 7b: Engineering time spent reviewing reticle inspections decreased by ∼90%

## 6. QUALITY: OPERATOR VS. ADAS

Operators correctly classify approx. 99.99% of all yield limiting defects however, human errors do occur (even with buddy checks) and occasionally cause expensive wafer loss. Eliminating human errors helps to maximize wafer yields and minimize avoidable wafer scrap. Figure 8 shows two examples where ADAS properly identified defects that had been deemed "passing" by operators as truly failing defects, saving potential yield-limiting reticle defects from reaching wafer production.

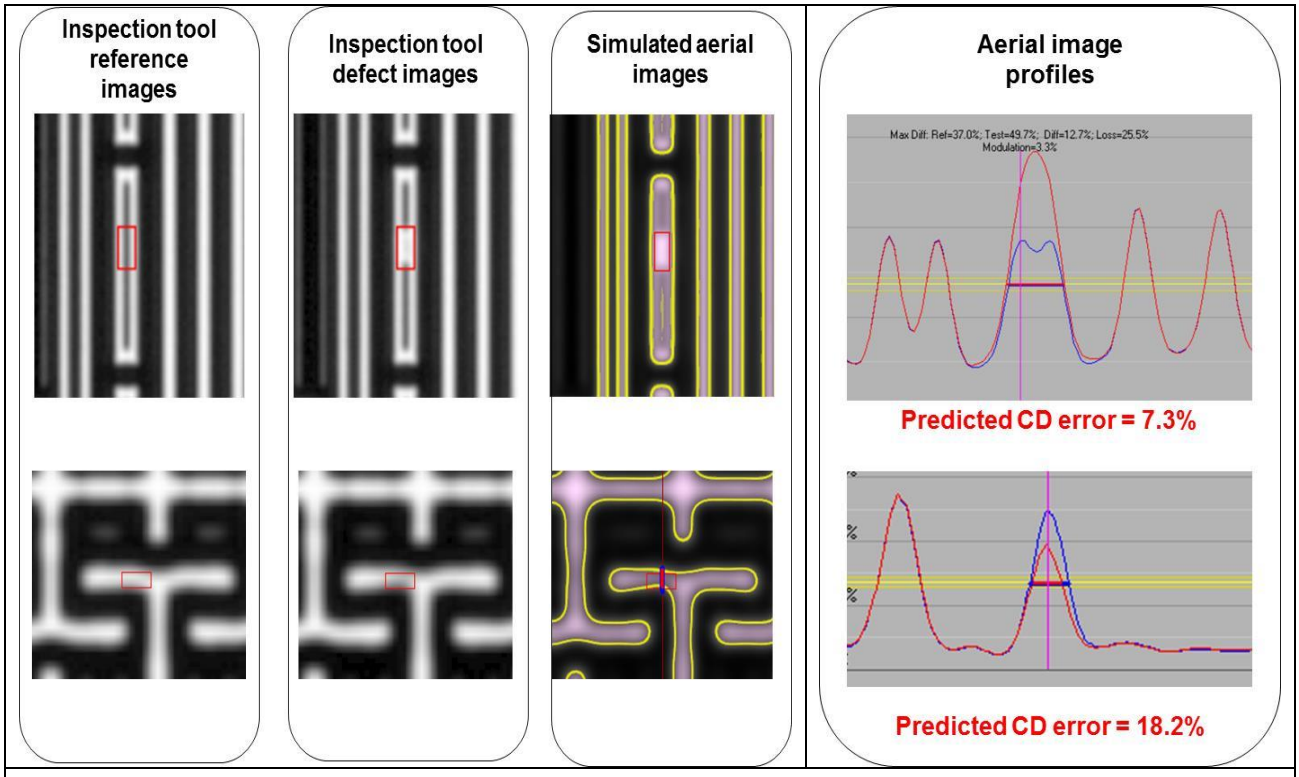


Figure 8: ADAS properly identified defects that had been passed by operators

## 7. TESTING SIMULATION AT 20NM NODE

The ADAS system has been in production in 28nm node and above in wafer fabs for over 18 months however, the system had yet to be tested at the 20nm node. The greatest concern was the ability to produce reliable defect simulation using the new freeform illumination sources. To test this capability, a 20nm production reticle that uses freeform illumination was modified with programmed defects and printed in order to create simulation data using freeform illumination conditions for comparison to actual wafer impact.

In this test, a 20nm production metal layer (referred to from here on as the "test" reticle) was modified by adding 41 real defects created by a state-of the art e-beam based reticle repair tool. Defects varied in size from 40nm to 240nm. A few examples of these programmed defects are shown in SEM reticle images in Figure 9. A test wafer was then printed using a standard focus/expose matrix. Coordinates of the defect locations were then compared to SEM images of the wafer after resist development as seen in the next section.

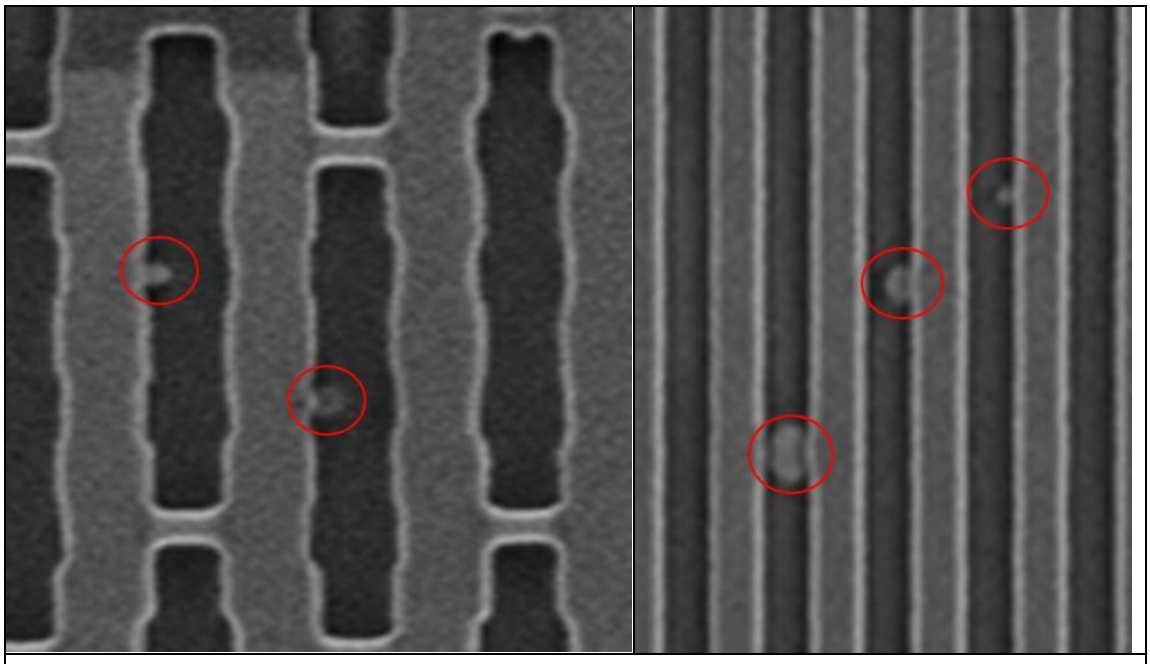

Figure 9: Two SEM test reticle images of embedded defects

## 8. PRINT TEST VERIFICATION

The wafer results from the test reticle were collected and compared with the results of the ADAS simulation model. A FEM (Focus Exposure Matrix) was shot with a 1.0mJ dose increment and a 15nm focus increment. Figure 10 shows some examples of the defects at BF (best focus) conditions. The top row in the figure contains reticle SEM images of the programmed defects. The second and third rows are SEM ADI (After Develop Image) wafer images showing the impact of the reticle defect. The fourth and fifth rows are ADAS simulation images showing the simulated impact of the reticle defects. As hoped, the ADAS simulation results show a good match to wafer print results, though in some cases as noted earlier, ADAS tends to over predict.

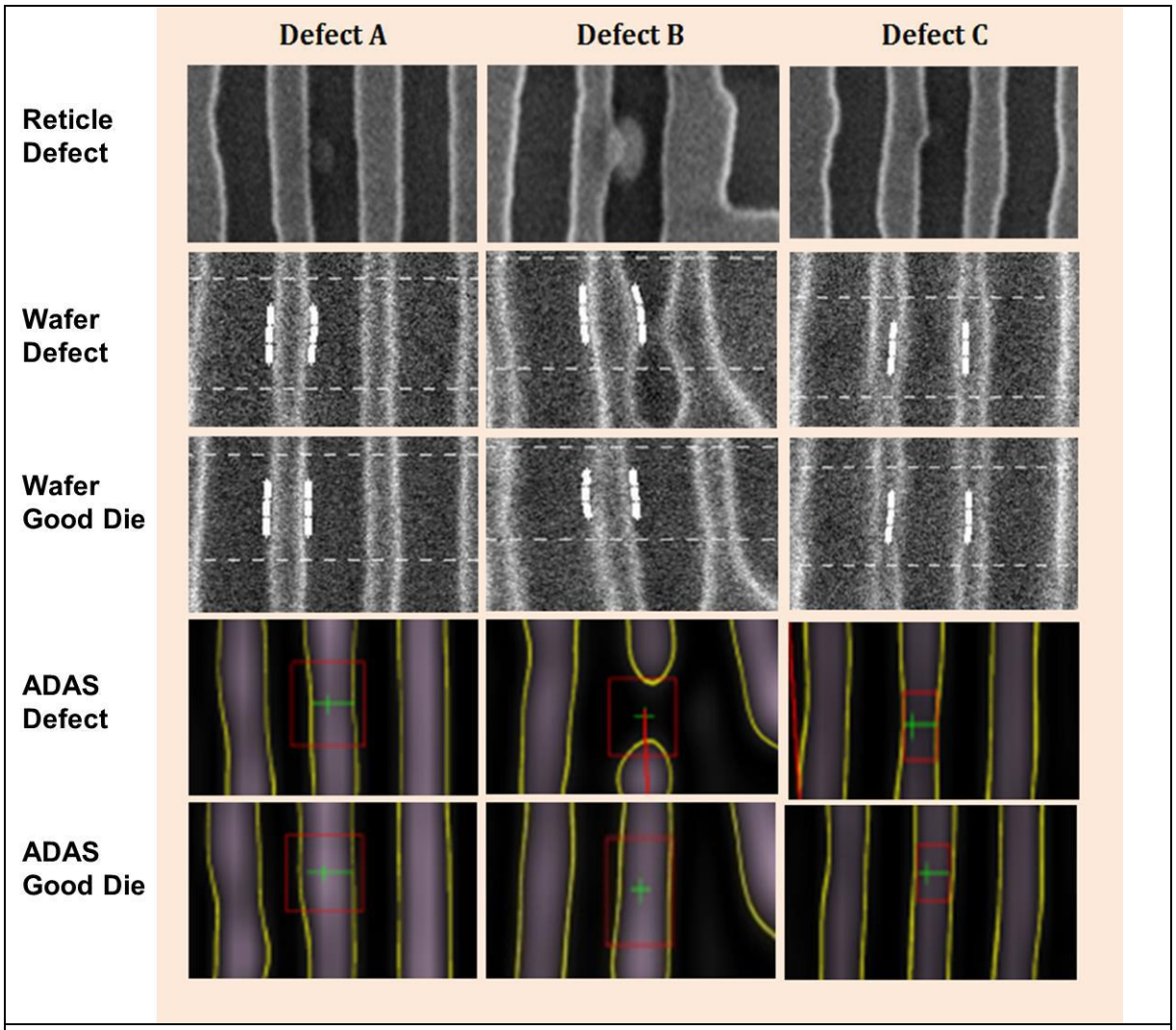


Figure 10: Comparison of ADAS simulation and SEM images of ADI wafer prints of programmed defects on the reticle

## 9. CORRELATION: ADAS VERSUS WAFER PRINT RESULTS

Correlation observed between ADAS and Wafer Prints is not perfect but reliable enough to differentiate between clearly passing and failing defects. Inspection tool pixel sizes are not shrinking in proportion to wafer feature sizes which adds to defect measurement noise. In this portion of our study, we found that the absolute CD error measured by ADAS tracks very well with the SEM-measured wafer CD percentage error enabling reliable defect dispositioning. Figure 11 shows that a relationship can be established between ADAS and wafer results to create a practical model for reticle engineers to disposition defects properly.

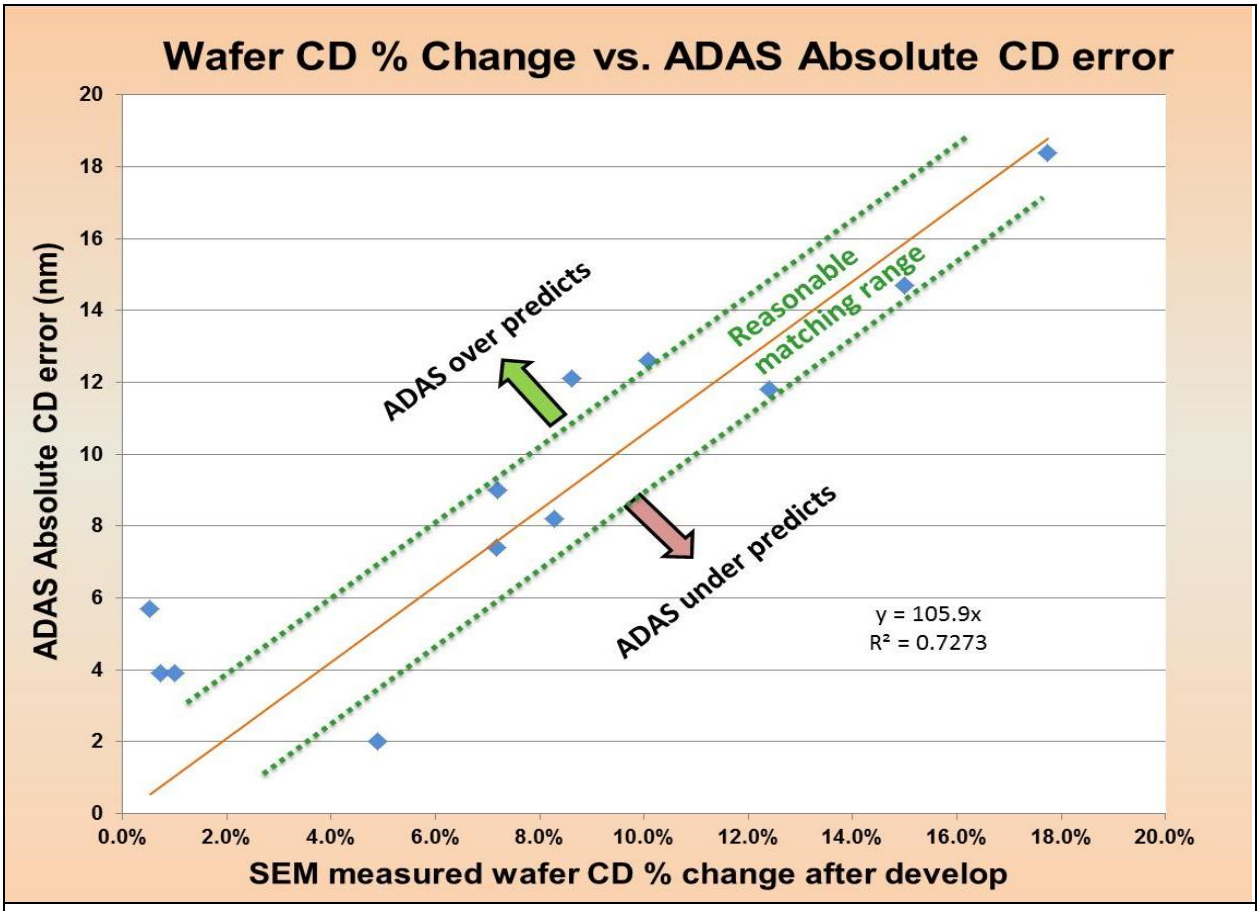


Figure 11: A model showing relationship between ADAS CD error and Wafer level CD change

## 10. CONCLUSIONS

- The Automatic Defect Analysis System (ADAS) eliminates wafer yield loss due to human reticle defect classification errors.
- ADAS has been shown to increase inspection tool fleet productivity by 8.6% averaged over 16 months.
- Engineering time spent reviewing reticle defects has been reduced 90% since ADAS release.
- Due to reliable simulation, ~50% more "on hold" reticles are being released directly to production, reducing expensive cleaning/repel/repair costs and time out of production.
- Current wafer print data of 20nm node programmed reticle defects show that ADAS reliably simulates 20nm node defects using free-form illumination sources.

## 11. PATH FORWARD

This team will continue testing ADAS 20nm node capabilities using both production and programmed defect test reticles. It will also perform a thorough comparison with AIMS for 20nm node freeform illumination to complete the link with the disposition criteria used at mask shop facilities and at the fab using wafer print test results. In addition, ADAS will be tested and implemented at next nodes (14nm and below) for defect classification and simulation.

## REFERENCES

[1] Sung Jae Ryu, et. al. "Increasing reticle inspection efficiency and reducing wafer print-checks using automated defect classification and simulation" SPIE Proc. Vol.8880, 88800D (2013)

[2] Shazad Paracha, Samy Bekka, Benjamin Eynon, et.al. "Evaluation of Dry Technology for Removal of Pellicle Adhesive Residue on Advanced Optical Reticles" Proc. SPIE Proc. of SPIE Vol. 8880, 88800M (2013)